



GAU 2644

PATENT  
Att'y Dkt: 2207/5913

6A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:

SAGER, ET AL.

SERIAL NO.: 09/745,549

FILED: DECEMBER 26, 2000

FOR SYSTEM AND METHOD FOR  
PARTIAL MERGES FOR SUB-  
REGISTER DATA OPERATIONS

EXAMINER: UNASSIGNED

ART UNIT: 2644

RECEIVED  
NOV 13 2001  
Technology Center 2600

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

Preliminary to examination of the above-identified application, please amend the application as follows:

IN THE SPECIFICATION:

Please replace the paragraph on page 2, beginning at line 6, with the paragraph shown below. A clean version of the replacement paragraph is attached hereto.

Typically, the merge occurs when the instruction is retired. For example, the Pentium® Pro P6 processor (manufactured by Intel Corporation of Santa Clara, California), one prior art processor supports 8 and 16 bit operations. To merge an 8 or 16 bit result with the unchanged bits of a register, ~~the P6~~ a prior art processor uses a Retired Register File (RRF). The RRF maintains copies of each of the eight physical registers of the x86. When an instruction is retired (which can occur well after the instruction was executed), the 8, 16, or 32 bit result of the instruction is transmitted to the RRF. Using its copy of the register in question, the RRF merges the result of the